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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,576	02/12/2004	Toshiharu Furukawa	ROC920030271US1	6152

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EXAMINER	
NADAV, ORI	
ART UNIT	PAPER NUMBER
2811	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/777,576	FURUKAWA ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-13,15-20 and 34-53* is/are pending in the application.

4a) Of the above claim(s) *9-13,20,36,38-42 and 49-51* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-8,15-19,34,35,37,43-48,52 and 53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/12/04,1/26/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-8, 15-19, 34-35, 37, 43-48 and 52-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth et al. (6,515,325) in view of Ochipinti et al. (2004/0027889).

Regarding claims 1 and 43, Farnworth et al. teach in figure 1 and related text a circuit comprising:

an interconnected plurality of semiconductor device structures arranged in an array (see figure 2I), each of said semiconductor device structures further comprising

a gate electrode 19 including a vertical sidewall and a gate dielectric disposed on the vertical sidewall,

at least one semiconducting carbon nanotube 22 extending substantially vertically between opposite first and second ends at a location adjacent to said vertical sidewall of said gate electrode,

a first contact 17 electrically coupled with said first end of said at least one semiconducting carbon nanotube,

and a second contact 21 electrically coupled with said second end of said at least one semiconducting carbon nanotube.

Farnworth et al. do not explicitly state that the array is characterized by a plurality of rows and a plurality of columns.

Ochipinti et al. teach that a memory device conventionally uses an array characterized by a plurality of rows and a plurality of columns (paragraph [0010]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an array characterized by a plurality of rows and a plurality of columns in Farnworth et al.'s device in order to simplify the processing steps of making the device by using conventional rows and columns array matrix.

Regarding claims 3-8, 34, 37, 44-48, Farnworth et al. teach said at least one semiconducting carbon nanotube is a single-wall semiconducting carbon nanotube, and

a plurality of semiconducting carbon nanotubes extending vertically at a plurality of locations adjacent to said vertical sidewall of said gate electrode (see figure 2I), wherein

said first contact includes a catalyst pad (by considering the first contact layer as layer 16, the catalyst pad is layer 16, see figure 2A and related text in column 4, lines 32-50) characterized by nanocrystals of a catalyst material effective for growing said at least one semiconducting carbon nanotube, wherein

said first end of said at least one semiconducting carbon nanotube incorporates an electrical-conductivity enhancing substance diffused from said catalyst pad into said first end during growth, and

an insulating layer disposed between said first contact 17 and said gate electrode 19 for electrically isolating said first contact from said gate electrode, and

an insulating layer disposed between said second contact 21 and said gate electrode for electrically isolating said second contact from said gate electrode.

Regarding the process limitations recited in claims 5-6 ("nanocrystals of a catalyst material effective for growing said at least one semiconducting carbon nanotube", and "an electrical-conductivity enhancing substance diffused from said catalyst pad into said first end during growth"), these would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claims 15-18, prior art teach a memory circuit comprising:

a plurality of word lines each electrically intreconnecting said gate electrode of each of said plurality of semiconductor device structurers located in a corresponding one of said plurality of rows of said array; and

a plurality of bit lines each electrically interconnecting said second contact of each of said plurality of semiconductor device structures located in a corresponding one of said plurality of columns of said array, wherein

each of said plurality of word lines comprises said gate electrode of each of said plurality of semiconductor device structures located in said corresponding one of said plurality of rows of said array, wherein

each of said plurality of bit lines comprises a conductive stripe electrically coupling said source of each of said plurality of semiconductor device structures located in a corresponding one of said plurality of rows of said array.

Regarding claims 19 and 52, prior art teach a substrate carrying said plurality of semiconductor device structures and characterized by a surface area viewed vertical to the substrate, said plurality of semiconductor device structures separated a space filled by a dielectric material. Prior art do not teach said space ranging from about 20 percent to about 50 percent of said surface area. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a space ranging from about 20 percent to about 50 percent of said surface area in prior art's device in order to reduce the size of the device and by optimizing the characteristics of the device.

Regarding claims 35 and 53, prior art teach a capacitor electrically coupled with said first contact.

Response to Arguments

Applicant argues that Farnworth fails to disclose or suggest "at least one semiconducting carbon nanotube extending substantially vertically between opposite first and second ends at a location adjacent to said vertical sidewall of said gate electrode", "a first contact electrically coupled with said first end of said at least one semiconducting carbon nanotube" and "a second contact electrically coupled with said second end of said at least one semiconducting carbon nanotube.", because the second "end" of the U shaped nanotube 22 is not electrically coupled with the drain 21 but with the source 17.

The phrase "an end of an element" does not limit the end (discontinuation) of the element to a specific x, y or z direction. The term "end" refers to any discontinuation of the element in any of the x, y or z directions. Therefore, in Farnworth's device, any point along the periphery of nanotube 22 can be called an "end". There is no requirement to limit the "end of the nanotube" to the specific direction as chosen and argued by applicant. Therefore, Farnworth et al. teach "at least one semiconducting carbon nanotube extending substantially vertically between opposite first and second ends at a location adjacent to said vertical sidewall of said gate electrode", "a first contact electrically coupled with said first end of said at least one semiconducting

carbon nanotube" and "a second contact electrically coupled with said second end of said at least one semiconducting carbon nanotube.", as claimed.

Applicant argues that Ochipinti et al. do not teach how the disclosed rows and columns of the array could be established and connected in Farnworth et al.'s device.

No secondary reference would disclose how to be incorporated in an unknown chosen primary reference. The examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it is conventional to use an array characterized by a plurality of rows and a plurality of columns in a memory device.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
3/17/07

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